II. Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

cleaning the surface of the substrate;

forming a thin insulate over the substrate;

depositing a high dielectric constant (high-k) material over the thin insulate;

performing a hydrogen-based anneal on the high-k material;

performing an oxygen-based anneal on the high-k material, wherein the hydrogen-based and oxygen-based anneals occur sequentially.

2. (Original) The method of claim 1 further comprising:

selecting a first temperature, a first pressure, and a first time for the hydrogen-based anneal; and

selecting a second temperature, a second pressure, and a second time for the oxygen-based anneal.

3. (Original) The method of claim 2 wherein the first temperature is selected from a range between about 500° C and about 1000° C, the first pressure is selected from a range between about 0.1 torr and about 760 torr, and the first time is selected from a range between about 10 seconds and about 10 minutes.

4. (Original) The method of claim 3 wherein the first temperature is about 800° C, the first pressure is about 40 torr, and the first time is about 1 minute.

5. (Original) The method of claim 2 wherein the second temperature is selected from a range between about 700° C and about 900° C, the second pressure is selected from a range between about 1 millitorr and about 10 torr, and the second time is selected from a range between about 1 second and about 300 seconds.

6. (Original) The method of claim 1 further comprising selecting a first chemical for the hydrogen-based anneal and a second chemical for the oxygen-based anneal, wherein the first and second chemicals are selected based on a chemical composition of the high-k material.

7. (Original) The method of claim 6 wherein the first chemical is selected from the group consisting of:

H_2;

NH_3; and

SiH_4.

8. (Original) The method of claim 6 wherein the second chemical is selected from the group consisting of:

O_2;

N_2O;

NO; and

D_2O.

9. (Original) The method of claim 1 wherein the high-k material is deposited using an atomic layer deposition (ALD) process.

10. (Original) The method of claim 9 wherein the high-k material is HfO_2, and wherein the method further comprises selecting an HfO_2 deposition temperature from a range between about 200° C and about 400° C, and selecting a deposition depth from a range between about 3 Angstroms and about 75 Angstroms.

11. (Original) The method of claim 10 wherein a plurality of cycles of the ALD process are performed until the selected deposition depth is attained.

12. (Original) The method of claim 1 wherein the substrate comprises diamond.

13. (Original) A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

placing a pseudo-substrate in a process reactor;

applying a loading treatment to the pseudo-substrate;

removing the pseudo-substrate from the process reactor;

placing a device substrate into the process reactor; and

forming a poly-silicon layer upon the device substrate.

14. (Original) The method of claim 13 wherein the pseudo-substrate comprises a material selected from the group consisting of:

silicon; and

diamond.

15. (Original) The method of claim 13 further comprising:

selecting a first temperature, a first pressure, and a first time for the loading treatment; and

selecting a second temperature, a second pressure, and a second time for the poly-silicon layer formation.

16. (Original) The method of claim 15 wherein the first temperature is selected from a range between about 550° C and about 750° C, the first pressure is selected from a range between about 0.1 torr and about 80 torr, and the first time is selected from a range between about 1 second and about 5 minutes.

17. (Original) The method of claim 16 wherein the first temperature is about 625° C, the first pressure is about 40 torr, and the first time is about 1 minute.

18. (Original) The method of claim 15 wherein the second temperature is selected from a range between about 700° C and about 900° C, the second pressure is selected from a range between about 1 millitorr and about 760 torr, and the second time is selected from a range between about 1 second and about 20 minutes.

19. (Original) The method of claim 13 further comprising selecting a chemical for the loading treatment.

20. (Original) The method of claim 19 wherein the chemical is selected from the group consisting of:

H_2;

NH_3; and

SiH_4.

21. (Original) The method of claim 13 wherein the loading treatment is performed within the same process environment as the poly-silicon formation.

22. (Original) The method of claim 13 wherein the loading treatment is performed within an individual process environment.

23. (Original) The method of claim 13 wherein the loading treatment employs a plasma.

24. (Original) A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

cleaning the surface of the substrate;

forming a thin insulate over the substrate;

depositing a high dielectric constant (high-k) material over the thin insulate;

performing a hydrogen-based anneal on the high-k material;

performing an oxygen-based anneal on the high-k material, wherein the hydrogen-based and oxygen-based anneals occur sequentially;

applying a loading treatment to the high-k material; and

forming a poly-silicon layer on the treated high-k material, wherein the loading treatment and poly-silicon deposition occur sequentially.

25. (Original) The method of claim 24 further comprising:

selecting a first temperature, a first pressure, and a first time for the hydrogen-based anneal;

selecting a second temperature, a second pressure, and a second time for the oxygen-based anneal.

selecting a third temperature, a third pressure, and a third time for the loading treatment; and

selecting a fourth temperature, a fourth pressure, and a fourth time for the poly-silicon layer formation.

26. (Original) The method of claim 25 wherein the first temperature is selected from a range between about 500° C and about 1000° C, the first pressure is selected from a range between about 0.1 torr and about 760 torr, and the first time is selected from a range between about 10 seconds and about 10 minutes.

27. (Original) The method of claim 26 wherein the first temperature is about 800° C, the first pressure is about 40 torr, and the first time is about 1 minute.

28. (Original) The method of claim 25 wherein the second temperature is selected from a range between about 700° C and about 900° C, the second pressure is selected from a range between about 1 millitorr and about 10 torr, and the second time is selected from a range between about 1 second and about 300 seconds.

29. (Original) The method of claim 25 wherein the third temperature is selected from a range between about 450° C and about 650° C, the third pressure is selected from a range between about 0.1 torr and about 80 torr, and the third time is selected from a range between about 1 seconds and about 5 minutes.

30. (Original) The method of claim 29 wherein the third temperature is about 500° C, the third pressure is about 40 torr, and the third time is about 2 minutes.

31. (Original) The method of claim 25 wherein the fourth temperature is selected from a range between about 700° C and about 900° C, the fourth pressure is selected from a range between about 1 millitorr and about 760 torr, and the fourth time is selected from a range between about 1 second and about 20 minutes.

32. (Original) The method of claim 24 further comprising selecting a first chemical for the hydrogen-based anneal, a second chemical for the oxygen-based anneal, and a third chemical for the loading treatment, wherein the first, second, and third chemicals are selected based on a chemical composition of the high-k material.

33. (Original) The method of claim 32 wherein the first chemical is selected from the group consisting of:

H_2;

NH_3; and

SiH_4.

34. (Original) The method of claim 32 wherein the second chemical is selected from the group consisting of:

O_2;

N_2O;

NO; and

D_2O.

35. (Original) The method of claim 24 wherein the high-k material is deposited using an atomic layer deposition (ALD) process.

36. (Original) The method of claim 35 wherein the high-k material is HfO_2, and wherein the method further comprises selecting a HfO_2 deposition temperature from a range between about 200° C and about 400° C, and selecting a deposition depth from a range between about 3 Angstroms and about 75 Angstroms.

37. (Original) The method of claim 35 wherein a plurality of cycles of the ALD process are performed until a selected deposition depth is attained.

38. (Original) The method of claim 24 wherein the loading treatment is performed within the same process environment of the poly-silicon formation.

39. (Original) The method of claim 24 wherein the loading treatment is performed within an individual process environment.

40. (Original) The method of claim 24 wherein the loading treatment employs a plasma.

41. (Original) The method of claim 24 wherein the substrate comprises diamond.

42. (Original) A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

cleaning the surface of the substrate;

forming a thin insulate on the substrate;

depositing a high dielectric constant (high-k) material upon the thin insulate;

performing an anneal on the high-k material;

applying a loading treatment upon the high-k material; and

forming a poly-silicon layer on the treated high-k material, wherein the anneal and poly-silicon deposition occur sequentially.

43. (Original) The method of claim 42 further comprising:

selecting a first temperature, a first pressure, and a first time for the loading treatment; and

selecting a second temperature, a second pressure, and a second time for the poly-silicon layer formation.

44. (Original) The method of claim 43 wherein the first temperature is selected from a range between about 450° C and about 650° C, the first pressure is selected from a range between about 0.1 torr and about 80 torr, and the first time is selected from a range between about 1 second and about 5 minutes.

45. (Original) The method of claim 44 wherein the first temperature is about 500° C, the first pressure is about 40 torr, and the first time is about 2 minutes.

46. (Original) The method of claim 43 wherein the second temperature is selected from a range between about 700° C and about 900° C, the second pressure is selected from a range between about 1 millitorr and about 760 torr, and the second time is selected from a range between about 1 second and about 20 minutes.

47. (Original) The method of claim 42 further comprising selecting a chemical for the loading treatment.

48. (Original) The method of claim 47 wherein the chemical is selected from the group consisting of:

H_2;

NH_3; and

SiH_4.

49. (Original) The method of claim 42 wherein the loading treatment is performed within the same process environment of the poly-silicon formation.

50. (Original) The method of claim 42 wherein the loading treatment is performed within an individual process environment.

51. (Original) The method of claim 42 wherein the loading treatment employs a plasma.

52. (Original) The method of claim 42 wherein the high-k material is deposited using an atomic layer deposition (ALD) process.

53. (Original) The method of claim 52 wherein the high-k material is HfO_2, and wherein the method further comprises selecting an HfO_2 deposition temperature from a range between about 200° C and about 400° C, and selecting a deposition depth from a range between about 3 Angstroms and about 75 Angstroms.

54. (Original) The method of claim 52 wherein a plurality of cycles of the ALD process are performed until a selected deposition depth is attained.

55. (Original) The method of claim 42 wherein the substrate comprises diamond.

56. (Withdrawn) A microelectronic device, comprising:

a doped well located in a susbtrate;

a gate structure, including:

a dielectric layer located over the doped well, the dielectric layer sequentially treated with a first, hydrogen-based anneal and a second, oxygen-based anneal; and

a semiconductor layer located over the dielectric layer; and

source/drain regions located in the doped well on opposing sides of the gate structure and extending partially between the dielectric layer and the doped well.

57. (Withdrawn) The microelectronic device of claim 56 wherein the substrate comprises diamond.

58. (Withdrawn) The microelectronic device of claim 56 further comprising a silicide layer located over the semiconductor layer.

59. (Withdrawn) The microelectronic device of claim 56 wherein the dielectric layer comprises a material selected from the group consisting of:

TaN;

TiN;

HfO_2; and

HfSiON.

60. (Withdrawn) The microelectronic device of claim 56 wherein the dielectric layer comprises a material selected from the group consisting of:

nickel silicide;

hafnium silicate;

nitrided hafnium silicate; and

hafnium aluminum oxide.